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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,693	09/23/2003	Maitreyee Mahajani	MA-105	2206
33971	7590	03/14/2005	EXAMINER	
MATRIX SEMICONDUCTOR, INC. 3230 SCOTT BOULEVARD SANTA CLARA, CA 95054			MANDALA, VICTOR A	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/668,693

Applicant(s)

MAHAJANI ET AL.

Examiner

Victor A. Mandala Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-59 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/3/04 & 8/9/04.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, multiple matrixes of SONOS transistors formed above one another and where the channel is formed above the gate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, 11, 12, 15, 16, 18-25, 27, 28, 31-41, & 43-53 are rejected under 35

U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,469,343 Miura et al.

2. Referring to claim 1, a SONOS-type device comprising: a tunneling dielectric, (Figure 2e #11), a dielectric charge storage layer, (Figure 2e #12, 13, 14, 15, & 16), in contact with the tunneling dielectric, (Figure 2e #11), the charge storage layer comprising a first dielectric film, (Figure 2e #12), and a second dielectric film, (Figure 2e #13), wherein the first and the second dielectric films, (Figure 2e #12 & 13), are formed of different materials, (Col. 8 Lines 7-17); and a blocking dielectric, (Figure 2e #17), in contact with the charge storage layer, (Figure 2e #12, 13, 14, 15, & 16).

3. Referring to claim 2, a SONOS-type device, wherein the first or the second dielectric film, (Figure 2e #12 & 13), comprises a dielectric material with a dielectric constant greater than or equal to 3.9, (Col. 8 Lines 7-17).

4. Referring to claim 3, a SONOS-type device, wherein the first dielectric film, (Figure 2e #12), comprises silicon nitride, silicon dioxide, hafnium oxide, aluminum oxide, zirconium oxide, or tantalum pentoxide, (Col. 8 Lines 7-17).

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5. Referring to claim 4, a SONOS-type device, wherein the first dielectric film comprises silicon nitride, (Figure 2e #12 & Col. 8 Line 5), and the second dielectric film comprises silicon dioxide, (Figure 2e #13 & Col. 8 Line 12).
6. Referring to claim 5, a SONOS-type device, wherein the charge storage layer further comprises a third dielectric film, (Figure 2e #14).
7. Referring to claim 6, a SONOS-type device, wherein the first dielectric film, (Figure 2e #12), and the third dielectric film, (Figure 2e #14), are formed of the same material, (Col. 8 Lines 7-17), and the second dielectric film, (Figure 2e #13), is interposed between the first, (Figure 2e #12), and third dielectric films, (Figure 2e #14).
8. Referring to claim 7, a SONOS-type device, further comprising a semiconductor channel, (Figure 2e #C), region in contact with the tunneling dielectric, (Figure 2e #11).
9. Referring to claim 8, a SONOS-type device, further comprising a gate electrode, (Figure 2e #6), in contact with the blocking dielectric, (Figure 2e #17).
10. Referring to claim 9, a SONOS-type device, wherein the gate electrode comprises polysilicon, (Figure 2e #6 and Col. 8 #25).
11. Referring to claim 11, a SONOS-type device, wherein the device is a portion of a memory array, (Col. 7 Lines 35 & Figure 9a).
12. Referring to claim 12, a SONOS-type device, wherein the memory array is a monolithic three-dimensional memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).
13. Referring to claim 15, a SONOS-type device, wherein the device is a portion of a memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).

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14. Referring to claim 16, a SONOS-type device, wherein the memory array is a monolithic three-dimensional memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).

15. Referring to claim 18, a SONOS-type device comprising: a tunneling dielectric, (Figure 2e #11), a dielectric charge storage layer, (Figure 2e #13, 14, 15, & 16), in contact with the tunneling dielectric, (Figure 2e #11), the charge storage layer, (Figure 2e #12, 13, 14, 15, & 16), comprising a first dielectric film, (Figure 2e #13), and a second dielectric film, (Figure 2e #14), wherein at least one of the first dielectric film, (Figure 2e #13), and the second dielectric film, (Figure 2e #14), does not comprise silicon nitride, (Figure 2e #13 & Col. 8 Line 9); and a blocking dielectric, (Figure 2e #17), in contact with the charge storage layer, (Figure 2e #13, 14, 15, & 16).

16. Referring to claim 19, a SONOS-type device, wherein the first dielectric film does not comprise silicon nitride, (Figure 2e #13 & Col. 8 Line 9).

17. Referring to claim 20, a SONOS-type device, wherein the first dielectric film comprises a dielectric material with a dielectric constant greater than or equal to 3.9, (Figure 2e #13 & Col. 8 Line 9).

18. Referring to claim 21, a SONOS-type device, wherein the first dielectric film comprises silicon dioxide, hafnium oxide, aluminum oxide, zirconium oxide, or tantalum pentoxide, (Figure 2e #13 & Col. 8 Line 9).

19. Referring to claim 22, a SONOS-type device, wherein the second dielectric film comprises silicon nitride, (Figure 2e #14 & Col. 8 Line 12-13).

20. Referring to claim 23, a SONOS-type device, further comprising a semiconductor channel region, (Figure 2e #C), in contact with the tunneling dielectric, (Figure 2e #11).

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21. Referring to claim 24, a SONOS-type device, further comprising a gate electrode, (Figure 2e #6) in contact with the blocking dielectric, (Figure 2e #17).
22. Referring to claim 25, a SONOS-type device, wherein the gate electrode comprises polysilicon, (Figure 2e #6 and Col. 8 #25).
23. Referring to claim 27, a SONOS-type device, wherein the device is a portion of a memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).
24. Referring to claim 28, a SONOS-type device, wherein the memory array is a monolithic three-dimensional memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).
25. Referring to claim 31, a SONOS-type device, wherein the device is a portion of a memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).
26. Referring to claim 32, a SONOS-type device, wherein the memory array is a monolithic three-dimensional memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).
27. Referring to claim 33, a SONOS-type device comprising: a tunneling dielectric, (Figure 2e #11); a blocking dielectric, (Figure 2e #17), a first dielectric charge storage film, (Figure 2e #16), in contact with the blocking dielectric, (Figure 2e #17), comprising a first material; and a second dielectric charge storage film, (Figure 2e #15), comprising a second material, the second charge storage film, (Figure 2e #15), in contact with the first charge storage film, (Figure 2e #16), wherein the second material, (Figure 2e #15 & Col. 8 Lines 26-27), and the first material, (Figure 2e #16 & Col. 8 Line 26), are not the same material, and wherein the first charge storage film, (Figure 2e #16), and the second charge storage film, (Figure 2e #15), are disposed between the tunneling dielectric, (Figure 2e #11), and the blocking dielectric, (Figure 2e #17).

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28. Referring to claim 34, a SONOS-type device, wherein the first material comprises a dielectric material with a dielectric constant greater than or equal to 3.9, (Figure 2e #16 & Col. 8 Line 26).

29. Referring to claim 35, a SONOS-type device, wherein the first material is silicon nitride, silicon dioxide, hafnium oxide, aluminum oxide, zirconium oxide, or tantalum pentoxide, (Figure 2e #16 & Col. 8 Line 26).

30. Referring to claim 36, a SONOS-type device, further comprising a third charge storage film, (Figure 2e #14) in contact with the second charge storage film, (Figure 2e #15).

31. Referring to claim 37, a SONOS-type device, further comprising a fourth charge storage film, (Figure 2e #13 & Col. 8 Line 9), in contact with the third charge storage film, (Figure 2e #14 & Col. 8 Lines 10-11), the first, (Figure 2e #16 & Col. 8 Line 26), and third charge storage films, (Figure 2e #14 & Col. 8 Lines 10-11), comprising the first material, and the second and fourth charge storage films, (Figure 2e #15 & 13 and Col. 8 Lines 9 & 26-27), comprising the second material.

32. Referring to claim 38, a SONOS-type device comprising: a tunneling dielectric, (Figure 2e #11); a blocking dielectric, (Figure 2e #17); a first dielectric charge storage film, (Figure 2e #12), disposed between the tunneling dielectric, (Figure 2e #11), and the blocking dielectric, (Figure 2e #17); and a second dielectric charge storage film, (Figure 2e #13), disposed between the tunneling dielectric, (Figure 2e #11), and the blocking dielectric, (Figure 2e #17), wherein at least one of the first charge storage film, (Figure 2e #12), and the second charge storage film, (Figure 2e #13), does not comprise silicon nitride, (Col. 8 Line 9), and wherein no material

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disposed between the tunneling dielectric, (Figure 2e #11), and the blocking dielectric, (Figure 2e #17), is a conductor or a semiconductor.

33. Referring to claim 39, a SONOS-type device, further comprising a channel region, (Figure 2e #C), in contact with the tunneling dielectric, (Figure 2e #11).

34. Referring to claim 40, a SONOS-type device, further comprising a gate electrode, (Figure 2e #6), in contact with the blocking dielectric, (Figure 2e #17).

40 41. Referring to claim 41, a SONOS-type device, wherein the gate electrode, (Figure 2e #6), is above the channel region, (Figure 2e #C).

35. Referring to claim 43, a SONOS-type device, further comprising a gate electrode, (Figure 2e #6), in contact with the blocking dielectric, (Figure 2e #17).

36. Referring to claim 44, a SONOS-type device, wherein: the first charge storage film, (Figure 2e #12 & Col. 8 Lines 5), is a first material, the second charge storage film, (Figure 2e #13 & Col. 8 Lines 9), is a second material, and the first material and the second material are not the same material.

37. Referring to claim 45, a SONOS-type device, wherein the first material is a dielectric material with a dielectric constant greater than or equal to 3.9, (Col. 8 Lines 5).

38. Referring to claim 46, a SONOS-type device, wherein the first material is silicon nitride, silicon dioxide, hafnium oxide, aluminum oxide, zirconium oxide, or tantalum pentoxide, (Col. 8 Lines 5).

39. Referring to claim 47, a method for making a SONOS-type memory cell, said method comprising the steps of: forming a semiconductor channel region, (Figure 2e #C); forming a tunneling dielectric, (Figure 2e #11); forming a blocking dielectric, (Figure 2e #17); forming a

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gate electrode, (Figure 2e #6); forming a first charge storage film, (Figure 2e #12), between the tunneling dielectric, (Figure 2e #11), and the blocking dielectric, (Figure 2e #17); and forming a second charge storage film, (Figure 2e #13), in contact with the first charge storage film, (Figure 2e #12), wherein at least one of the first charge storage film, (Figure 2e #12), and the second charge storage film, (Figure 2e #13), is not silicon nitride; and wherein the first charge storage film, (Figure 2e #12), is in contact with the blocking dielectric, (Figure 2e #17).

40. Referring to claim 49, a method, wherein the gate electrode, (Figure 2e #6), is over the channel region, (Figure 2e #C).

41. Referring to claim 50, a method, wherein the SONOS-type memory cell is a portion of a memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).

42. Referring to claim 52, a method, wherein the first charge storage film or the second charge storage film is between about 10 and about 190 angstroms thick, (Figure 2e #12 & 13 & Col. 8 Lines 5-6 & 9-10, where 15 nm = 150 Angstroms).

43. Referring to claim 51, a method, wherein the memory array is a monolithic three-dimensional memory, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).

44. Referring to claim 53, a memory array comprising a SONOS-type cell, said cell comprising: a tunneling dielectric, (Figure 2e #11), a dielectric charge storage layer, (Figure 2e #12, 13, 14, 15, & 16), in contact with the tunneling dielectric, (Figure 2e #17), the charge storage layer, (Figure 2e #12, 13, 14, 15, & 16), comprising a first dielectric film, (Figure 2e #12 & Col. 8 Line 5), and a second dielectric film, (Figure 2e #13 & Col. 8 Line 9), wherein the first and the second dielectric films are formed of different materials; and a blocking dielectric, (Figure 2e #17), in contact with the charge storage layer, (Figure 2e #12, 13, 14, 15, & 16),

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wherein the array is a nonvolatile memory array, (Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No.

6,469,343 Miura et al.

45. Referring to claim 1, a SONOS-type device comprising: a tunneling dielectric, (Figure 2e #11), a dielectric charge storage layer, (Figure 2e #12 & 13), in contact with the tunneling dielectric, (Figure 2e #11), the charge storage layer comprising a first dielectric film, (Figure 2e #12), and a second dielectric film, (Figure 2e #13), wherein the first and the second dielectric films, (Figure 2e #12 & 13), are formed of different materials, (Col. 8 Lines 7-17); and a blocking dielectric, (Figure 2e #17), in contact with the charge storage layer, (Figure 2e #12 & 13).

46. Referring to claim 17, a SONOS-type device, wherein the charge storage layer is between about 30 and about 200 angstroms thick, (Figure 2e #12 & 13 & Col. 8 Lines 5-6 & 9-10, where 15 nm = 150 Angstroms).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10, 42, & 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,469,343 Miura et al. in view of U.S. Patent No. 6,797,604 Chan et al.

47. Referring to claim 10, a SONOS-type device, wherein the gate electrode comprises tungsten, (Chan et al. Col. 2 Lines 54-55 and see + below).

+ Miura et al. discloses the claimed invention except for the gate electrode being made out of tungsten, but Chan et al. does in Col. 2 Lines 54-55. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the gate electrode out of tungsten, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

48. Referring to claim 42 and 48, a SONOS-type device, wherein the channel region is above the gate electrode, (Chan et al. Col. 2 Lines 54-55 and see ++ below).

++ Miura et al. teaches all of the claimed matter in claims 42 and 48, but is silent on the channel being formed above the gate, but Chan et al. does in Col. 2 Lines 54-55 wherein there is a backgate. It would have been obvious to one having skill in the art at the time the invention was made to form a channel above a gate instead of beneath, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japiske, 86 USPQ 70

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It is also well known that a semiconductor can be rotated and that channel can be positioned above the gate. A basic example could be looked at as placing a mobile phone on its face, where in the channel could be above the gate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 13, 14, 26, 29, & 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,469,343 Miura et al. in view of U.S. Patent No. 6,682,973 Paton et al.

49. Referring to claims 13, 26, and 29, a SONOS-type device, wherein the semiconductor channel region comprises polysilicon, (Paton et al. Col. 7 Lines 3-7 and see +++ below).

+++ Miura et al. discloses the claimed invention except for the channel being made out of polysilicon, but Paton et al. does in Col. 7 Lines 3-7. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the channel out of polysilicon, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

50. Referring to claims 14 and 30, a SONOS-type device, wherein the semiconductor channel region comprises mono-crystalline silicon, (Paton et al. Col. 7 Lines 3-7 and see ++++ on the next page).

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++++ Miura et al. discloses the claimed invention except for the channel being made out of mono-crystalline silicon, but Paton et al. does in Col. 7 Lines 3-7. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the channel out of mono-crystalline silicon, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 54-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,469,343 Miura et al. in view of U.S. Patent Application Publication No. 2002/0028541 Lee et al.

51. Referring to claim 54, a monolithic three-dimensional memory array, (Miura et al. Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a), comprising a plurality of SONOS-type memory cells, each cell comprising: a tunneling dielectric, (Miura et al. Figure 2e #11), a dielectric charge storage layer in contact with the tunneling dielectric, (Miura et al. Figure 2e #11), the charge storage layer comprising a first dielectric film, (Miura et al. Figure 2e #12), and a second dielectric film, (Miura et al. Figure 2e #13 & Col. 8 Line 9), wherein at least one of the first dielectric film, (Miura et al. Figure 2e #12 & Col. 8 Line 5), and the second dielectric film,

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(Miura et al. Figure 2e #13), does not comprise silicon nitride; and a blocking dielectric, (Miura et al. Figure 2e #17), in contact with the charge storage layer, (Miura et al. Figure 2e #12, 13, 14, 15, & 16), wherein the memory array comprises at least two levels of SONOS-type memory cells, one level formed vertically over the other, (See ** below).

** Miura et al. teaches all of the claimed matter in claim 54 and 55, but is silent on the memory array having two levels of SONOS-type memory cells, where one level is formed on top of the other. Lee et al. does teach the missing element, which can be seen in Lee et al.'s Figures 52 and 69 and is further taught in Paragraphs 0283-0285. It would have been obvious to one having skill in the art to arrange the memory cell arrays on top of each other for the mere convenience of spatial conservation and larger memory capacity, which has been the leading trend in semiconductor technology. The design is also a mere duplication of parts, which has also been found to be obvious to one having skill in the art, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. vs. Bomis Co* 193USPQ8

52. Referring to claim 55, a memory cell comprising: a channel region; and a tunneling oxide grown by an in situ steam generation process, (See *** below), the tunneling oxide, (Miura et al. Figure 2e #11), in contact with the channel region, (Miura et al. Figure 2e #C), wherein the memory cell is a portion of a monolithic three dimensional memory array, (Miura et al. Col. 7 Lines 35, Col. 8 Lines 44-48, & Figure 9a), comprising at least two levels of memory cells, one level formed vertically over the other, (See ** above).

*** Initially, and with respect to claim 55, note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Fitzgerald*, 205 USPQ 594, 596 (CCPA);

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In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

53. Referring to claim 56, a memory cell further comprising: a blocking oxide, (Miura et al. Figure 2e #17); and a dielectric charge storage layer, (Miura et al. Figure 2e #12, 13, 14, 15, & 16), in contact with the blocking oxide, (Miura et al. Figure 2e #17), and the tunneling oxide, (Miura et al. Figure 2e #11).

54. Referring to claim 57, a memory cell, wherein the dielectric charge storage layer comprises: a first dielectric charge storage film comprising a first material, (Miura et al. Figure 2e #12 & Col. 8 Line 5); and a second dielectric charge storage film comprising a second material, (Miura et al. Figure 2e #13 & Col. 8 Line 9), wherein the first material and the second material are not the same material.

55. Referring to claim 58, a memory cell, wherein the first material is silicon nitride, silicon dioxide, hafnium oxide, aluminum oxide, zirconium oxide, or tantalum pentoxide, (Miura et al. Col. 8 Line 5).

56. Referring to claim 59, a memory cell, wherein the in situ steam generation process is performed at a temperature of between about 750 degrees Celsius and about 1050 degrees Celsius, (See *** above).

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9568. **NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800**

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VAMJ
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